14th MRAM Global Innovation Forum

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December 8, 2022

14th MRAM Global Innovation Forum 2022

IEEE MAGNETICS

Sessions		Topics	Speakers
08:40-09:00: Welcome & Introduction (B. Dieny, K. Garello, E.S. Jung)			
MRAM in Industry I (chair: tbd)	09:00	Status and Outlook of eMRAM Technology	Tae Young Lee *Samsung* 
	09:30	N16 Embedded STT-MRAM Technology For RAM-like Application	Allen Wang *TSMC* 
	10:00	STT-MRAM and Beyond For High Performance Memory Applications	Vinayak Bharat Naik *Global Foundries* 
10:30-10:50 Break			
MRAM in Industry II (chair: tbd)	10:50	High-Speed Read and Low-Power Write Operation of STT-MRAM for Advanced Technology Nodes	Tomoya Saito *Renesas Electronics* 
	11:20	High Performance and Density STT-MRAM For Mission-Critical Applications	Yiming Huai *Avalanche Tech.* 
	11:50	Development Of SOT-MRAM Technology	Ming Yuan Song *TSMC* 
12:20-14:00 Break			
STT / SOT / VCMA developments (chair: tbd)	14:00	Double Spin-Torque Magnetic Tunnel Junctions for Sub-ns Switching	Guohan Hu *IBM* 
	14:30	Progress On VCMA, SOT, And VG-SOT Technologies For High Performance Memory Applications	Kaiming Cai *IMEC* 
Emerging MRAM concepts (chair: tbd)	15:00	In-Memory Computing With MRAM	Seungchul Jung *SAIT* 
	15:30	Magneto-electric Spin Orbit (MESO) Logic Device for Energy Efficient Computing	Punyashloka Debashi *Intel* 
	16:00	Ferroelectric Spin Orbit Devices for Ultralow Power Computing	Laurent Vila *Spintec* 
16:30-17:00 Break			
Panel Discussion	17:00 18:00	New technologies beyond existing STT-MRAM and benefits in the marketplace Moderator: Jack Guedj (*Numem*) Panelists: Seung Kang (*Adeia*), Daniel Worledge (*IBM*), Daniele Leonelli (*Huawei*), Simon Bertolazzi (*Yole*), Joe O'Hare (*Everspin*)	
18:00 Closing remarks			

Tae Young Lee

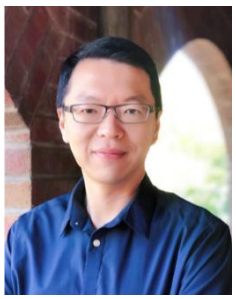
Principal Engineer,

Samsung Semiconductor

Dr. Tae Young Lee is a Principal Engineer of eMRAM Process Architecture Team in Foundry Business at Samsung Electronics. He has 13 years of academic research and industry development with MTJ stack engineering and device characterization. Prior to joining Samsung Electronics, he has multiple experience to develop advanced MRAM technology development and bring new MRAM product to market for both Standalone and Embedded memory. Since he joined Samsung Electronics in 2021, he has mainly contributed to the development for non-volatile RAM (nvRAM) product by using 28/14 nm embedded MRAM technology.

Status and Outlook of eMRAM Technology

Embedded non-volatile memory (eNVM) is used in various microcontroller unit (MCU) products for code/data storage. eFlash has been the mainstream eNVM technology, serving a variety of MCU products for more than 20 years. However, as eFlash faces scalability challenges beyond 28 nm, major foundries have developed emerging eNVM technologies such as MRAM, RRAM, and PRAM. As of today, all three major foundries are mass-producing eMRAM wafers in the segment of wearable and IoT applications. In this talk, we review the current status of eMRAM technology, highlighting the benefits of eMRAM as an eNVM platform technology as compared to the other emerging eNVM. We also discuss how recent market megatrends in automotive and edge AI would drive technological advance in eMRAM technology, creating greater opportunities beyond MCU markets.



Allen Wang

Senior Technical Manager,

TSMC

Allen Wang is a Senior Technical Manager of Embedded Technology Division at TSMC, where he leads the development of MTJ device design. He has 18 years industry experience on MRAM technology development and specializes in MTJ stack and MRAM integration. He currently focuses on RAM-like STT-MRAM development for AIoT and automotive applications. Prior to joining TSMC, he was Senior Manager at TDK-Headway contributing to perpendicular MTJ development for Flash-like STT-MRAM. He received Ph.D. in Material Science and Engineering from National Tsing Hua University in 2004 and holds over 80 MRAM-related US issued patents.

N16 Embedded STT-MRAM Technology for RAM-like Application

STT-MRAM is emerging as the leading candidate among various embedded memory technologies due to high performance such as scalability, excellent endurance, low power consumption and non-volatility. We previously reported a fully functional N16 Embedded STT-MRAM as Flash-like application for automotive-grade MCU products. To expand the range of application for STT-MRAM, we have moved our development focus from Flash-like MRAM toward RAM-like application. Herein, a fully functional high-yield N16 MRAM Macro with fast write speed and good endurance to support RAM-like applications is demonstrated. We will present our most recent device data by tuning the MTJ film stack along with an optimized etching scheme to achieve fast write speed (20ns) with decent endurance up to 1E+10. Furthermore, the advanced RAM-like MTJ device also possesses an excellent thermal stability compatible with standard Wafer-on-Wafer (WoW) process for 3D IC products.

Vinayak Bharat Naik

MRAM device lead,

GLOBAL FOUNDRIES

Vinayak Bharat Naik has received Ph.D. degree in Physics from National University of Singapore in 2011 and Executive MBA from SP Jain School of Global Management (expected in 2022). He is currently a MRAM Device lead at GLOBALFOUNDRIES (2014 to present), Singapore. Prior joining to GLOBALFOUNDRIES, he was working as a Scientist at Agency for Science, Technology and Research (A*STAR), Singapore (2011-2014) on conventional (high-density) and voltage-controlled STT-MRAM development. He has published 50+ technical papers in international journals/conferences and holds 25+ U.S. patents in the field of Non-volatile memory and sensor technologies.

STT-MRAM and Beyond for High Performance Memory Applications

In the on-going era of artificial intelligence (AI), Internet of Things (IoT) and autonomous vehicles (AV), the semiconductor industry has actively been developing emerging non-volatile memory (NVM) technologies. Among all the NVMs, Spin-Transfer-Torque (STT-MRAM) technology has proven to be a viable technology solution to replace embedded flash in advanced microcontroller units (MCU) and

microprocessor units (MCU) – thanks to STT-MRAM's robust device performance, fast read and write performances with high endurance and solder reflows compatibility. To support such broad range of products with single technology platform, it is crucial to evaluate STT-MRAM reliability and understand the trade-offs among MTJ device performances to optimize MRAM for targeted applications. In this talk, the status of 22FDX® embedded MRAM technology for industrial-grade MCU & IOT applications, and the potential of MRAM for next-generation high-performance memory & neuromorphic applications will be presented.

Tomoya Saito

Senior Manager,

Renesas Electronics

Tomoya Saito is a Senior Manager of Memory IP Technology Development Team in Renesas Electronics Corporation. He is currently responsible for the development of embedded STT-MRAM with a focus on macro IP characteristics and reliability. He has more than 20 years of experience in embedded Flash memory technology for both consumer and Auto applications. Prior to joining Renesas, he was a device engineer in a Flash technology vender. He received Ph.D. degree in Electronics Engineering from Osaka University in Japan.

High-speed read and low power write operation of STT-MRAM for advanced technology nodes

IoT and AI technology are powering a paradigm shifts toward a smart society. In the process of this shift, microcontroller unit (MCU) is playing a major role in a wide range of applications with secure and high-performance operation in home automation, robotics, and medical applications as well as intermittent low-energy operation in IoT endpoint applications. MCUs with embedded flash memory (eFlash) have the advantages in terms of security and faster boot load time without initial program code loading from external flash memories. Endpoint MCUs with eFlash also contribute to low power operation supplied with batteries or energy harvesting sources. On the other hand, it has become increasingly difficult to provide eFlash at advanced technology nodes such as 2Xnm and beyond because of its complex process steps, low affinity with advanced CMOS process, and need for high voltage transistors to support 10V-class write/erase voltage.

Accordingly, embedded STT-MRAM (eMRAM) has been expected to replace eFlash due to fewer additional masks, BEOL process, and lower write voltage. However, there are several challenges in accelerating read speed, which enhances performance of MCUs with eMRAM, and realizing low energy write to expand new MCU applications. These are due to intrinsic MRAM's characteristics of smaller read margin especially in high temperature and the variation in write current.

In this paper, a high-precision boosted cross-couple sense amplifier (BCC-SA) is introduced to achieve 5.1ns random read access time at high temperature of 125°C [1]. In addition, a novel self-termination write schemes [2] and a variable parallel bit write (VPBW) sequence are proposed to enhance the advantage of eMRAM and realize both 65-69% lower write energy and 5.8MB/s fast rewrite throughput [1]. These achievements using 2Xnm and/or 1Xnm process technology will enable us to continuously provide advanced MCU products with embedded non-volatile memory to expand new MCU applications.

The authors gratefully acknowledge the contributions of TSMC.

[1] T. Shimoi et al., VLSI2022, pp.134-135. [2] T. Ito et al., IEDM 2021, pp. 2.2.1-2.2.4.

Yiming Huai

CTO & VP of Technology and Foundry Business,

Avalanche Technology

Dr. Yiming Huai serves as CTO & VP of Technology and Foundry Business, at Avalanche Technology, a world's leading provider of STT MRAM technology and products. He leads Avalanche STT MRAM technology/product development and manufacturing in collaboration with top-tier foundries. Prior to joining Avalanche, Dr. Huai was co-founder, board member and CTO of Grandis, Inc, a pioneer in the Spin Transfer Torque MRAM (STT MRAM). Grandis was acquired by Samsung in 2011. While at Grandis, Yiming successfully raised more than $30 M in private and government funding. He led the team to first demonstrate spin transfer switching in magnetic tunnel junctions, creating a foundation for STT MRAM commercialization. Prior to Grandis, Huai served as Sr. Director of Thin Film of Manufacturing at Read-Rite Corporation (now Western Digital) from 1996 to 2002, where he led the development and volume production of industry leading GMR heads for hard disk drives. He previously worked as a Staff Scientist at the Lawrence Livermore National Laboratory (LLNL) and as a Post-Doctoral Fellow at the National Research Council in Ottawa, Canada. He received M.S. and Ph.D. degrees, both in Physics, from the University of Montreal in Canada. He has authored or co-authored more than 120 papers, holds more than 180 issued patents. He has delivered over 90 keynote and invited speeches on STT MRAM technology.

High Performance and Density STT MRAM For Mission-Critical Applications

STT-MRAM has been standing out from emerging NVM technologies as a leading solution for both embedded flash and SRAM replacements at advanced nodes beyond 28 nm. On standalone applications, STT-MRAM's outstanding features of high-speed performance (<40 ns), practically unlimited endurance, high-temp data retention and inherent radiation immunity enable high reliability memories for mission-critical applications. In this invited talk, we will present silicon data of 1-8 Gb packaged dies which are manufactured with 22 nm nodes at UMC foundry. Traditionally mission critical systems relied upon multiple volatile & non-volatile memory devices to support functions such as boot, code execution, data monitoring and logging. With the release of the highest density and high reliability STT-MRAM products combined with standard SRAM type interface and timing, we provide a revolutionary solution of unified MRAM memory array that simplifies mission critical systems architecture.

Guohan Hu

Distinguished Research Staff Member,

IBM

Guohan Hu is a Distinguished Research Staff Member and manager of the MRAM Materials and Devices group at the IBM T. J. Watson Research Center. Guohan received her Ph.D. degree in Materials Science and Engineering from Cornell University in 2002. She received a Bachelor of Engineering degree in Materials Science & Engineering, and a Bachelor of Economics degree in Enterprise Management from Tsinghua University in 1997. Guohan's research interests are in MRAM materials and devices, magnetic oxide thin films, and magnetic recording media. Guohan is an editor of IEEE Electron Device Letters and a fellow of the IEEE.

Double Spin-torque Magnetic Tunnel Junctions for sub-ns switching

We introduce a new two terminal device structure – double spin-torque magnetic tunnel junction (DS-MTJ) to reduce the switching current of STT-MRAM devices. A DS-MTJ consists of a bottom reference layer, a tunnel barrier, a free layer, a non-magnetic spacer layer and a top reference layer. Utilizing the spin-torques generated from both reference layers, we demonstrated a 2x reduction in switching current, compared to the control structure without any TMR degradation. When combined with low RA tunnel barriers, write-error-rate (WER) of 1E-6 was achieved in hundreds of DS-MTJ devices with 250 ps write pulses and tight distributions. We compare the DS-MTJ device high-speed switching performance to published results from state-of-the-art three terminal Spin-Orbit-Torque (SOT) MRAM devices and show a 10x reduction in switching current density (Jc) and 3-10x reduction in power consumption for devices with similar energy barriers (Eb).

MingYuan Song

Principal Engineer and Technical Manager,

TSMC

MingYuan Song joined TSMC (Hsinchu, Taiwan) in 2017 as principal engineer. He is a graduate of National Taiwan University, where he majored in Physics Ph. D. Prior to TSMC, he was postdoc at the institute of Physics at Academia Sinica, Taiwan. During his tenure at TSMC, he was assigned to advanced spintronics metrology and the sponsor of SOT-MRAM project.

Development of SOT-MRAM technology

We demonstrated an 8Kb SOT-MRAM array which achieves 1ns field-free switching with low switching current density (JSW) 68 MA/cm^2 and 0 write error rate (8Kb), high retention (>>10 years) and high endurance 7e12 cycles. The unique tungsten-based composite SOT channel material (SCM) was developed to provide high spin-Hall angle (~0.6) and low resistivity (160μΩ-cm) with 400℃ thermal budget. The 8Kb SOT-MRAM array showed good read window and array yield by optimized MTJ etching process. The SOT-MRAM array has, high retention (>>10 years) and high endurance 7e12 cycles are demonstrated as well.

Kaiming Cai

Research Scientist,

IMEC

Kaiming Cai received the Ph.D. in Physics from the University of Chinese Academy of Sciences (Beijing, China) in 2017. From 2017 to 2020, he was a research fellow at the National University of Singapore (NUS). Since 2021, he has joined the Department of Compute and Memory Device (CMD) at IMEC as a research scientist, focusing on the research and development of magnetic memory technologies. Since 2011, he has been studying magnetism and spintronics, specifically the spin-orbit torque (SOT) effect and its applications in MRAM. His main research interests are ultrafast and field-free switching of SOT devices.

Progress on VCMA, SOT, and VG-SOT technologies for high performance memory applications

Memory is one of the critical components in electronic systems for data storage and processing. Among the memories, magnetic memories, such as STT, SOT, and VCMA-MRAMs, exhibit the advantages of fast speed, non-volatile, good endurance, scalability, and CMOS compatibility. To date, STT-MRAM has become a mature technology in recent years with the major foundries announcing large volume production of embedded STT-MRAM products [1]. SOT-MRAM has been highlighted as a potential candidate for SRAM replacement due to its ultrafast switching and better endurance, to overcome the long access time and reliability issues of STT-MRAM. However, the three-terminal configuration and high switching current in SOT-MRAM adversely impact its reliability and bit-cell area, thus limiting the integration density. To further reduce the switching energy, VCMA-MRAM has been demonstrated with low power and ultrafast switching by voltage. In addition, the proposed VG-SOT MRAM, combining SOT and VCMA effects in one system, enables selective operations between multi-pillar MTJ devices with low switching currents and high integration density.

In this talk, I will present some latest progress at IMEC on the developments of VCMA, SOT, and VG-SOT MRAM technologies. For SOT-MRAM, we developed the BEOL-compatible hybrid free layer [2], enabling high switching efficiency and thermal budget, and demonstrated the concepts for field-free switching through bending current and hybrid SOT track layers. We also achieve a high VCMA coefficient > 100 fJ/Vm in the VCMA-MRAM [3]. Moreover, for the first time, we experimentally demonstrated the selective operations of multiple MTJs on a shared SOT track by VG-SOT, enabling >30% reduction of switching current and less transistors for high density integration [4].

[1] J.G. Alzate et al., IEEE IEDM 2.4.1-2.4.4 (2019).
[2] S. Couet et al., IEEE Symp. on VLSI Circuit, T11 (2021).
[3] R. Carpenter et al., IEEE IEDM 17.6.1-17.6.4 (2021)
[4] K. Cai et al., IEEE Symp. On VLSI Technology, 375-376 (2022).

Seungchul Jung

Principal Researcher,

Samsung Advanced Institute of Technology

Seungchul Jung received the B.S. (magna cum laude, minor: chemistry) and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2006 and 2014, respectively. In 2014, he joined the Samsung Advanced Institute of Technology (SAIT), Suwon, South Korea, where he is currently a principal researcher. He was involved in the development of wireless battery chargers and power management integrated circuits for implantable devices until early 2019. He is currently involved in the design of in-memory computing circuits and computing architectures for neuromorphic processors.

In-memory computing with MRAM

The sensational success of artificial intelligence (AI) has been made possible by performing the neural net computation in digital processors. At the same time, there is an intense on-going search for new processor architectures that borrow analog techniques to drastically improve the energy efficiency of the neural net computing. The most celebrated example is the in-memory computing architecture based on the memory crossbar array, which stores neural net weights and performs neural net algebra in an analog fashion. Its superb power saving has nucleated a wealth of efforts to realize the crossbar array using various non-volatile memories (NVMs). So far, no crossbar array has been built with spin transfer torque magnetoresistive random access memory (MRAM), despite its excellent precision, speed, stability, and endurance. The key challenge has been its low resistance that would consume a large power in the conventional crossbar array arrangement, defeating the purpose of the crossbar array. We realized the first-ever MRAM crossbar array, which was published on Nature. We overcame the low-resistance issue by innovating a new crossbar array architecture that uses resistance summation.

Punyashloka Debashis

Research Engineer,

Intel

Punyashloka Debashis received B.Tech and M.Tech in Electrical Engineering from the Indian Institute of Technology Kanpur and Bombay in 2012 and 2014 respectively, and Ph.D. in Electrical and Computer Engineering from Purdue University in 2020, where he was part of the early investigation into computing using spintronics based probabilistic bits.

He joined Intel Corporation in 2020 as a Research Engineer in the Components Research division in Hillsboro, Oregon. He is responsible for the integration and characterization of beyond-CMOS devices and for mentoring joint research programs with universities on nanotechnology and exploratory devices. From 2014-2017, he was a Mary I. Williams fellow at Purdue University. Between 2018-2020, he served as an Ambassador for Purdue Discovery Park. Punya was one of the three winners of Purdue 3-minute thesis award in 2019. In 2022, he won a divisional recognition award at Intel for the

demonstration of magnetoelectric switching at 150 mV. He has 30 publications in refereed journals and conferences in spintronics and nanoelectronics, and 25 issued or submitted patents in spintronic, ferroelectric and magnetoelectric devices.

Magneto-Electric Spin Orbit (MESO) logic device for energy efficient computing

The development of next generation of energy efficient beyond-CMOS computing hardware will be based on low switching voltage and higher functionality logic devices. Recent advances have demonstrated the feasibility of such a logic device by utilizing magnetoelectric (ME) materials to switch a nanomagnet and using spin-orbit (SO) effects to read out its state. This talk will present some of these key experimental advances.

Material and process innovations that enabled the progression from 6V to 500 mV voltage driven switching of CoFe magnetization direction in functional magnetoelectric devices utilizing the perovskite BiFeO3 as the ME element will be presented. Following this, the material and device parameters affecting the spin-orbit readout of the magnetization state would be discussed and the continuous improvement in the read-out signal levels in the recent years will be presented. The first demonstration of a fully integrated MESO device will be shown, although while not yet at the target performance.

Our most recent experimental results, showing 150 mV voltage-driven switching of a ferromagnet exchange-coupled to 6-nm-thick lanthanum-doped BiFeO3 and less than 2 ns switching of this material's polarization at room temperature will be presented.

Finally, some of the key challenges for enabling the design of high functionality beyond-CMOS logic circuits such as lowering the switching voltage to <100 mV with fast switching dynamics, improving the readout voltage >100 mV, and improving the device endurance will be summarized.

Laurent Vila

Senior Researcher,

Spintec, CEA

Dr. Laurent Vila is a Researcher at Spintec, CEA, and an expert in the design, nanofabrication and characterization of innovative spintronics devices. He has pioneer several studies on the spin to charge inter conversion by Spin Hall and of the inverse Rashba Edelstein effects, including in oxides 2DEG's and topological insulators. He has led several projects related to the spin to charge interconversion by the spin orbit effect and has recently discovered the ferroelectric control of the spin to charge current interconversion. He has contributed to the development of the MRAM R&D line at Spintec. He is author of more than 160 peer-reviewed papers and 8 patents.

Ferroelectric spin orbit devices for ultralow power computing

We present a new kind of spintronic/ferroelectric device, the FerroElectric Spin-Orbit (FESO) device. We demonstrate that the spin-to-charge conversion due to the spin-orbit coupling can be directly controlled in sign, in a remanent way, through the ferroelectric polarization. This constitute the birth of a ferroelectric spintronics, which could result in a drastic reduction of the power consumption of non-volatile spintronic devices, down to the attojoule range, and at low operating voltages.

While spintronics has traditionally relied on ferromagnetic metals as spin generators and detectors, the efficient spin-charge interconversion enabled by spin-orbit coupling in non-magnetic systems has drawn a considerable interest in recent years. It allows extending the field of spintronics beyond CoFeB and MgO-based devices, towards classes of materials exhibiting other types of magnetoelectric coupling, such as ferroelectricity. This provides new opportunities for creating spin-based devices, such as the MESO device proposed recently by Intel [1], which relies on the writing of a magnetic information through magnetoelectric coupling, and of its reading by spin-charge interconversion.

Here, by controlling directly the sign of the interconversion through a ferroelectric state, it is possible to merge the writing and reading blocks, and to avoid the need for switching a magnetic state using multiferroicity. Moreover, by merging spintronics and ferroelectricity, the FESO device circumvents several drawbacks of competing technologies, such as the destructive reading of Fe-RAMs, or the sensitivity to external magnetic fields of Magnetic Tunnel Junctions (MTJs) and MESO devices.

The spin orbit coupling allows interconverting spin and charge currents both in the bulk of materials by spin Hall effect, or at interfaces by Rashba-Edelstein effect. We demonstrate its ferroelectric control in two classes of materials: two-Dimensional Electron Gases (2DEGS) appearing at oxides surfaces or interfaces [2, 3], and ferroelectric Rashba semiconductors [4]. The demonstration of a non-volatile ferroelectric control of the conversion in two classes of materials constitute an important argument for the feasibility of the FESO device. Both these classes of materials present specific challenges and assets for their industrial integration, and could constitute the future platform of ultralow power computing.

[1] S. Manipatruni et al., "Scalable energy-efficient magnetoelectric spin–orbit logic", Nature 565, 35–42 (2019).

[2] D. C. Vaz et al, "Mapping spin–charge conversion to the band structure in a topological oxide two-dimensional electron gas", Nature Materials 18, 1187–1193 (2019)
[3] P. Noel et al., "Non-volatile electric control of spin–charge conversion in a SrTiO3 Rashba system", Nature 580, 483–86 (2020).
[4] S. Varotto et al., "Room-temperature ferroelectric switching of spin-to-charge conversion in germanium telluride", Nature Electronics 4, 740-747 (2021).

PANEL DISCUSSION:

New technologies beyond existing STT-MRAM and benefits in the market place

Moderator: Jack Guedj (*CEO,* **Numem**)

Panelists:

Seung Kang

Vice President of Semiconductor Strategy,

Adeia

Dr. Seung Kang has recently joined Adeia as Vice President of Semiconductor Strategy. Till September 2022, he was Director of Engineering at Qualcomm Technologies, Inc. where he built and led the Advanced Memory Program which included pioneering STT-MRAM and spintronic device for mobile systems. He also led the foundation logic IP development for 5, 4, and 3 nanometer nodes. He received B.S. and M.S. degrees from Seoul National University, Korea, and his Ph.D. degree from the University of California at Berkeley. Prior to Qualcomm, he worked at Lucent Technologies Bell Laboratories as Distinguished Member of Technical Staff and Lawrence Berkeley National Laboratory as a materials scientist. Dr. Kang is a prolific inventor with ~250 US Patents granted. He has contributed to publishing >100 papers. He was a Distinguished Lecturer for the IEEE Electron Device Society from 2014-2018, and has served as Specially Appointed Visiting Professor, Center for innovative Integrated Electronic Systems, Tohoku University, Japan.

Daniele Leonelli

Senior Scientist,

Huawei

Bio to updated

Simon Bertolazzi

Senior Technology & Market analyst,

Yole

Simone Bertolazzi, PhD is a Senior Technology & Market analyst, Memory, at Yole Intelligence, part of Yole Group, working with the Semiconductor, Memory & Computing division. As member of the Yole's memory team, he contributes on a day-to-day basis to the analysis of memory markets and technologies, their related materials, device architectures and fabrication processes.
Previously, Simone carried out experimental research in the field of nanoscience and nanotechnology, focusing on emerging semiconducting materials and their opto-electronic device applications. He (co-) authored more than 20 papers in scientific journals and was awarded the Marie Curie Intra-European Fellowship. Simone obtained a PhD in physics in 2015 from École Polytechnique Fédérale de Lausanne (Switzerland), where he developed flash memory cells based on heterostructures of two-dimensional materials and high-κ dielectrics. Simone earned a double M. A. Sc. degree from Polytechnique de Montréal (Canada) and Politecnico di Milano (Italy), graduating cum laude.

Daniel C. Worledge

Distinguished Research Staff Member,

IBM

Dr. Worledge received a BA with a double major in Physics and Applied Mathematics from UC Berkeley in 1995, receiving the Department Scholar Award in physics and the Dorothea Klumpke Roberts Prize in mathematics. He then received a PhD in Applied Physics from Stanford University in 2000, with a thesis on spin-polarized tunneling in oxide ferromagnets, measuring the largest tunneling spin-polarization in (LaSr)MnO3 and the first negative tunneling spin-polarization in SrRuO3. After joining the Physical Sciences Department at the IBM T. J. Watson Research Center as a Post-doc in 2000, he became a Research Staff Member in 2001, inventing and developing Current-in-Plane Tunneling as a fast turn-around measurement method for magnetic tunnel junctions. In 2003, Dr. Worledge became the manager of the MRAM Materials and Devices group, and in 2013 he became Senior Manager of MRAM. In 2015 he was promoted to Distinguished Research Staff Member. He has worked on developing Toggle and then Spin-Transfer-Torque MRAM, including discovering perpendicular magnetic anisotropy in CoFeB|MgO and using these materials to make the first practical perpendicularly magnetized tunnel

junctions. Daniel led the IBM team to demonstrate the first integrated perpendicular Spin-Transfer-Torque MRAM, with ultra-low bit error rate. His current research interests include magnetic devices and their behavior at small dimensions, and new hardware approaches to machine learning. Dr. Worledge has received four IBM Outstanding Technical Achievement Awards, three IBM Outstanding Innovation Awards, and the IBM Research Client Award.

Joe O'Hare

Senior Director of Marketing,

Everspin

Joe has had a rewarding career working in the semiconductor industry at companies such as TI, Lucent Microelectronics, Agere Systems and now Everspin Technologies. He has held a variety of engineering, marketing and executive positions with a focus on developing products for the storage industry, both magnetic and solid state.

At Everspin Technologies, Joe has held roles in sales and marketing since 2011.

As Senior Director of Marketing at Everspin Technologies, Joe is leading the effort to define and launch a new class of STT-MRAM memory that is targeted at storage and industrial applications where performance and persistence are valued. He also has led the efforts to build a strong distributor network of our products and has led promotion efforts of the product and company at customers and the industry overall.

14th MRAM Global Innovation Forum

San Francisco, 8 December 2022

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Chair: Bernard Dieny, Luc Thomas and Kevin Garello

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